REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1-69 remain pending. Claims 1-69 have been rejected.

In this response, claims 1 and 34 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

REJECTIONS TO THE SPECIFICATION

The title of the invention has been rejected for not being descriptive.

Applicants have amended the title to overcome the Examiner's rejection.

REJECTIONS UNDER 35 U.S.C. 102

Claims 1-2, 4-7, 9-20, 23-30, 32-35, 37-40, 42-53, 56-63, 65-66 and 68 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,446,198 to Sazegari ("Sazegari").

Amended claim 1 reads as follows:

A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
      receiving a string of bits;
      generating a plurality of indices using a plurality of segments of bits in the string of bits;
      <u>looking up simultaneously a plurality of entries from a plurality of independent look-up tables using the plurality of indices, wherein each of said plurality of look-up tables is separate and distinct from others of said plurality of look-up tables</u>; and
      combining the plurality of entries into a first result;
      <u>wherein the above operations are performed in response to the microprocessor receiving the single instruction</u>. (emphasis added)

Sazegari discloses a completely different method than claimed by Applicants. Sazegari discloses performing multiple permute operations with at least one select operation on a data table (col. 7, lines 35-45). Each of the permute operations is performed on the pair of vectors containing the data within the data table (col. 7, lines 45-50). More specifically, Sazigari discloses dividing the data table into a number of smaller tables. Each of the smaller tables consists of two data vectors, which constitutes operands for the permute instruction (col. 2, lines 17-23). Importantly, Sazegari discloses simultaneously performing a number of lookup operations in such a single smaller table (Figure 2, col. 3, line 64-col. 4, line 3). In particular, Sazegari discloses that

> For table lookup operations, the permute instruction can be used to perform 16 simultaneous lookup operations on a 32-byte entry table. FIG. 4 illustrates such a table 34, which consists of two 16-byte vectors, data1 and data2. Each vector can be stored in one register of the CPU. The permute instruction can be used to simultaneously read 16 values from these two vectors, in accordance with index values in a register 36, and store the 16 output results in sequential order in another register 38.

(col. 4, lines 24-32, col. 4, lines 59-66) (emphasis added).

Thus, Sazegari merely discloses the permute instruction to simultaneously look up entries from portions of the single table. In contrast, claim 1 refers to looking up simultaneously a plurality of entries from a plurality of independent look-up tables using the plurality of indices, wherein each of said plurality of look-up tables is separate and distinct from others of said plurality of look-up tables.

Because Sazegari fails to disclose all limitations of claim 1, Applicants respectfully submit that claim 1 is not anticipated under 35 U.S.C. § 102(e) by Sazegari.

Because claims 2-69 contain related limitations, Applicants respectfully submit that claims 2-69 are not anticipated under 35 U.S.C. § 102(e) by Sazegari.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 3, 8, 21-22, 31, 36, 41, 54-55, 64 and 69 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari, as applied above.

As set forth above, Sazegari fails to disclose looking up simultaneously a plurality of entries from a plurality of independent look-up tables using the plurality of indices, wherein each of the plurality of look-up tables is separate and distinct from others of said plurality of look-up tables, as recited in claim 1.

Therefore, Applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103(a) over Sazegari.

Given that claims 3, 8, 21-22, 31, 36, 41, 54-55, 64 and 69 contain related limitations, Applicants respectfully submit that claims 3, 8, 21-22, 31, 36, 41, 54-55, 64 and 69 are not obvious under 35 U.S.C. § 103(a) over Sazegari.

Claim 67 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari, as applied above, in view of U.S. Patent No. 5,526,501 to Shams ("Shams").

It is respectfully submitted that Sazegari does not teach or suggest a combination with Shams, and Shams does not teach or suggest a combination with Sazegari. Sazegari teaches a vectorized table lookup by a single processor. Shams, in contrast, teaches accessing the look up tables by the array of processors (col. 1, lines 15-col. 2, line 15). It would be impermissible hindsight, based on Applicants own disclosure, to combine Sazegari and Shams.

Furthermore, even if Sazegari and Shams were combined, such a combination would lack the following limitations of claim 1: looking up simultaneously a plurality of entries from a plurality of independent look-up tables using the plurality of indices, wherein each of the plurality of look-up tables is separate and distinct from others of the plurality of look-up tables.

Therefore, Applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103(a) over Sazegari in view of Shams.

Given that claim 67 contains related limitations, Applicants respectfully submit that claim 67 is not obvious under 35 U.S.C. § 103(a) over Sazegari in view of Shams.
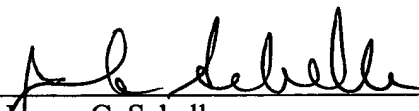
CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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